until a delay element delay time after the evaluate clock instructs the dynamic logic to reset.

PLEASE RE-WRITE PAGE 4, PARAGRAPH 1 (A.K.A. LINES 2-10) AS FOLLOWS:

FIG. 1 is a schematic illustration of a static to dynamic logic interface that produces a monotonic output. In FIG. 1, IN is the input signal from static logic. OUT is the output signal that may be connected to dynamic logic. CK is the inverse of the dynamic logic evaluate clock. In the embodiment shown in FIG. 1, when CK is low it is the dynamic logic evaluate phase. CK is input to delay element **104**. The output of delay element is a delayed version of CK called CKD. Delay element **104** may be as simple as an even number of inverters. CK is also connected to the clock input of a transparent latch **102** and CKD is connected to an enable input of transparent latch **102**.

PLEASE RE-WRITE PAGE 4, PARAGRAPH 2 (A.K.A. LINES 11-17) AS FOLLOWS:

The net result of feeding CK and CKD the clock input and the enable input, respectively, of transparent latch **102** is a static to dynamic logic interface that is open until the inverse of the dynamic logic evaluate clock falls. This static to dynamic logic interface also remains closed until a delay element delay after the dynamic logic evaluate clock falls. These properties help prevent hold time problems while providing timing benefits in an easy to construct solution with low implementation cost.

IN THE CLAIMS:

CANCEL CLAIMS 1-9 AND 13-16.

RE-WRITE CLAIMS 10 AND 11 AS FOLLOWS: